

Terabit™

Enterprise M.2 110mm PCIE/NVMe Solid State Drive

Data Sheet

Terabit Technology

Revision History

Version	Date	Changes	Note
V001	2016-04-28	Release	

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Contents

1. Product Features.....4

2. Overview.....5

3. Interface.....5

4. Physical Dimension.....6

5. PIN Description.....8

 5.1 PIN Location.....8

 5.2 Signal Description.....8

6. Power Consumption.....9

7. Product Reliability.....10

 7.1. Wear Leveling.....11

 7.2 ECC.....11

 7.3 MTBF.....11

 7.4 Bad-block Management.....11

 7.5 S.M.A.R.T Function.....11

 7.6 TRIM Function.....11

8. Performance.....12

9. Cache.....12

10. NVMe Command List.....13

11. Certifications.....14

12. Ordering Information.....15

13. Contact Information.....15

1. Product Features

Interface	PCIe Gen3 x 4
Form Factor	M.2 22110
Dimension	110.0 x 22.0 x 3.8 ±0.1(mm)
Capacity	NAND MLC: 240GB~960GB
Performance	Read up to 2500MB/s Write up to 1350MB/s
Power Supply	D/C 3.3V± 5%
Operating Temperature	Standard: 0~+70°C Enterprise: -20~+70°C
Weight	<30g
Storage Temperature	-40~+85°C
Shock	Non-operating 1500G peak, 0.5ms Operating 50G peak, 11ms
Vibration	20Hz~80Hz/1.52mm ~ 80Hz-2000Hz/20G X,Y,Z axis/60min for each
Drop	80cm free falling
Bending	≥20N / Hold 1min/5 times
Burn-in Test	36 Hours
Max. Power Consumption	Sequential Reading 5.11W Sequential Writing 6.92W Idle 0.4W
MTBF	2,000,000 Hours
Features	<ul style="list-style-type: none"> - Enhanced endurance by dynamic/static wear-leveling - Support dynamic power management - Support S.M.A.R.T function - Automatic Bad-block Management - Support TRIM and NCQ(Native Command Queuing) Command - Support BCH ECC 66bits/1024bytes - Low Power Management
Data Retention	@25°C: 10 years
Certification	CE/FCC/RoHS

2. Overview

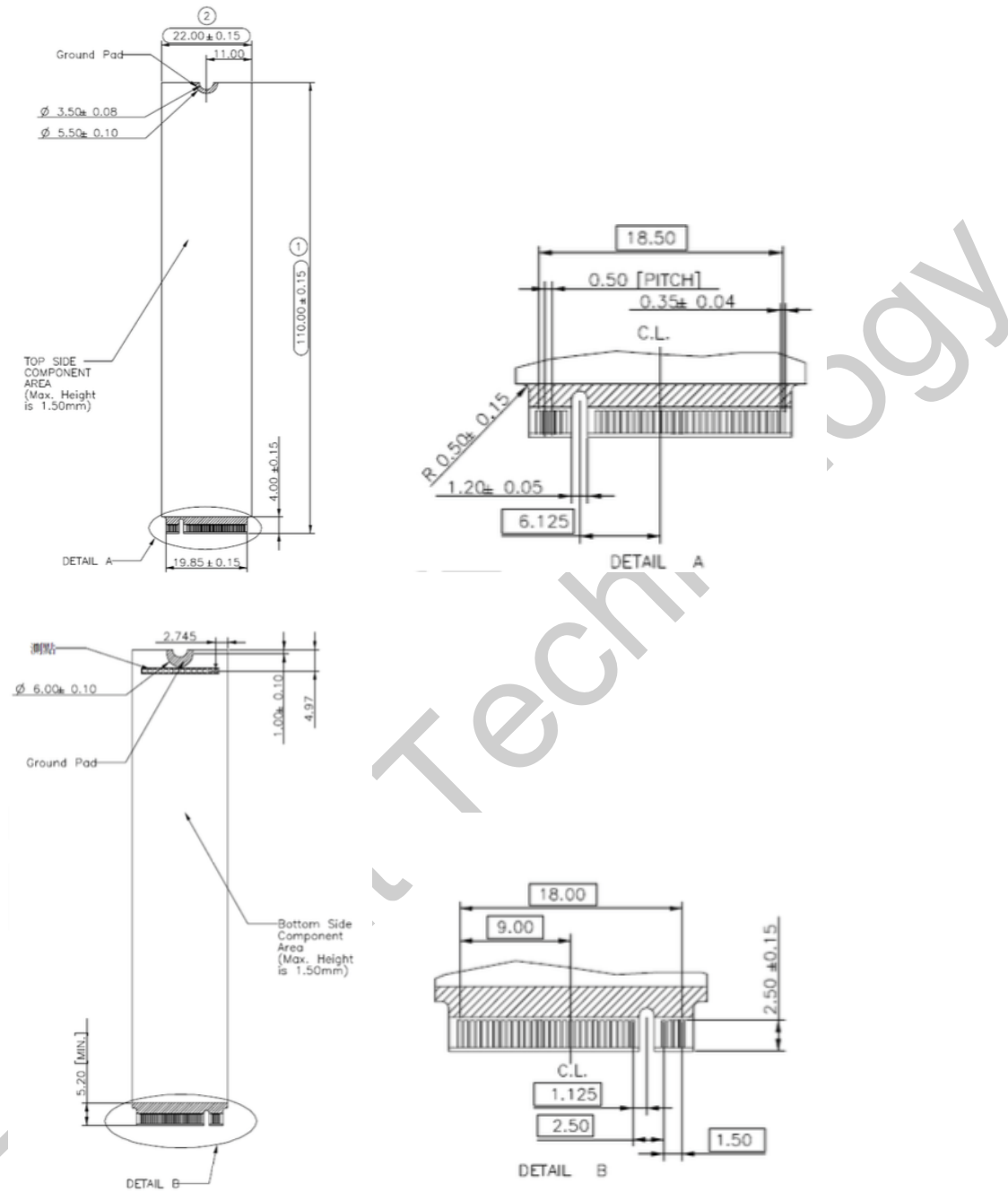
Terabit M.2 110mm PCIE SSD fully consists of semiconductor devices using original Toshiba Toggle NAND MLC Flash, which provide high reliability and high performance for data storage. Terabit M.2 110mm PCIE SSD has standard interface for different applications, and fully conforms to the same mechanical and mounting requirements as standard rotating disk drives. This series of products are designed for premium applications that require both strong reliability and high capacity while installing room is limited such as Embedded Computer, Panel Computer, Enterprise Server, Media Player, Ultra-book and Workstations. With up to 960GB capacity on NAND MLC Flash Terabit M.2 110mm PCIE SSD totally goes through a variety of proofing tests such as Shock Test, Vibration Test, Burn-in Test, and Twisting Test. Well proved under -20~+70°C temperature and equipped with Power Failure Protect and Over Load Protect, this series of products can work smoothly under Enterprise environments.

3. Interface

Terabit M.2 110mm PCIE Solid State Drive complies PCIe Gen3.0 x 4

- Compliant with NVMe 1.2
- Compatible with PCIe I/II/III x 4 interface
- Support up to queue depth 64K
- Support power management ASPM/PCI-PM L0s, L1.2 and L1.2

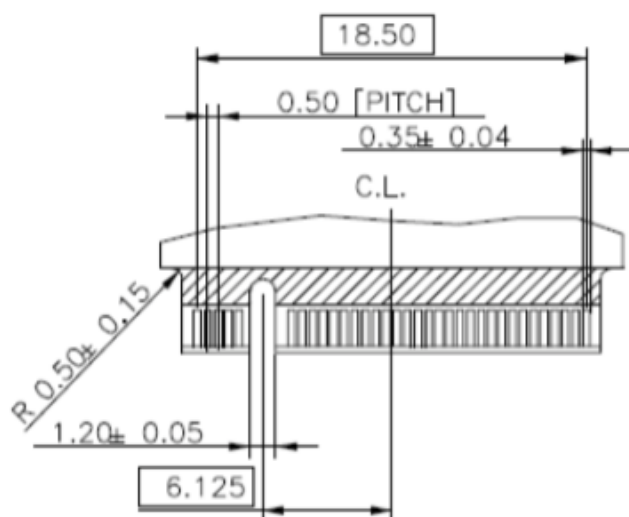
4. Physical Dimension



Parameter	Value	Unit
Length	110.0	mm
Width	22.0	mm
Height	3.80	mm

5. PIN Description

5.1 PIN Location



5.2 Signal Description

Pin#	Type	Description	Pin#	Type	Description
1	GND	Ground	2	3.3V	3.3V Source
3	GND	Ground	4	3.3V	3.3V Source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec	6	No connect	
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec	8	No connect	
9	GND		10	LED1#(O)	
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec	12	3.3V	3.3V Source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec	14	3.3V	3.3V Source
15	GND		16	3.3V	3.3V Source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec	18	3.3V	3.3V Source
19	PETp2	PCIe TX Differential signal defined	20	No connect	

		by the PCI Express M.2 spec			
21	GND		22	No connect	
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec	24	No connect	
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec	26	No connect	
27	GND		28	No connect	
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec	30	No connect	
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec	32	No connect	
33	GND		34	No connect	
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec	36	No connect	
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec	38	No connect	
39	GND		40	No connect	
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec	42	No connect	
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec	44	No connect	
45	GND		46	No connect	
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec	48	No connect	
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec	50	PERST#(I)(O/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND		52	CLKREQ#(I/O)(O/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Substates.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express	54	PEWAKE#(I/	PCIe PME Wake. Open Drain with

		M.2 spec.		O)(0/3.3V)	pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.	56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND		58	Reserved for MFG CLOCK	
59	Module Key		60	Module Key	
61	Module Key		62	Module Key	
63	Module Key		64	Module Key	
65	Module Key		66	Module Key	
67	No connect		68	SUSCLK(32K Hz) (I)(0/3.3V)	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module.
69	PEDET (NC-PCIe)	Host I/F Indication; No Connect for PCIe.	70	3.3V	3.3V Source
71	GND		72	3.3V	3.3V Source
73	GND		74	3.3V	3.3V Source @0.5 Amps
75	GND				

6. Power Consumption

Capacity	Idle	Read	Write	Unit
240GB	0.40	4.44	3.37	W
480GB	0.40	4.89	4.81	W
960GB	0.40	5.11	6.92	W

7. Product Reliability

NAND MLC Flash:

Capacity	Endurance Total Bytes Written	Data Retention	MTBF	Warranty
240GB	Up to 350TB	@25°C >10 Years	2 Million Hours	3 Years Limited
480GB	Up to 700TB			
960GB	Up to 1400TB			

*Total Bytes Written= 【(Flash P/E cycle) x (number of bits in drive)】 /WAI
WAI=1.428704724

7.1 Wear-Leveling

Terabit M.2 110mm PCIE SSD supports both static and dynamic wear-leveling technology. These two algorithms guarantee each block of flash memory at same level of erase cycles to improve lifetime limitation of NAND based storage.

7.2 ECC

ECC (Error Correction Code): Enhanced configurable BCH ECC engine. Terabit M.2 110mm PCIE SSD implements the BCH ECC Algorithm, which is one of the most powerful ECC algorithms in the industry. This algorithm can correct up to 60 random bit errors in each 512 bytes.

7.3 MTBF

Mean time between failures (MTBFs) for the SSD can be predicted based on the component reliability data using the methods referenced in the SR-332 reliability prediction procedures for electronic equipment, the prediction result for this SSD is more than 2,000,000 hours.

7.4 Bad-block Management

Terabit implements an efficient bad block management algorithm into the SSD to detect factory produced bad blocks as well as those that develop over the lifetime of the device. This process is completely transparent to the user through the use of S.M.A.R.T. command tools, i.e., the user will not be aware of the existence of the bad blocks during operation.

7.5 S.M.A.R.T Function

S.M.A.R.T stands for Self-Monitoring, Analysis and Reporting Technology. This technology enables the PC to predict the future failure of hard disk drives. Through the S.M.A.R.T. system, Terabit M.2 110mm PCIE SSD incorporates a suite of advanced diagnostics that monitor the internal operation of the drive and provide an early warning for many types of potential problems. When a potential problem is detected, the SSD can be repaired or replaced before any data is lost or damaged.

7.6 TRIM Function

Terabit Solid State Drive equips built-in TRIM function, it helps collect and clean data garbage when the system in an idle situation, which keeps the system in a high performance status even after long-term using.

8. Performance

Capacity	Sequential R(max)	Sequential W(max)	IOPS Read (max)	IOPS Write (max)
240GB	2300MB/s	650MB/s	270,000	180,000
480GB	2400MB/s	1200MB/s	280,000	200,000
960GB	2500MB/s	1350MB/s	300,000	250,000

9. Cache

Cache	DDR2	DDR3	Capacity
Support	/	Yes	/

10. NVMe Command List

Admin Commands

Opcode	Command description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download

Admin Commands-NVM Command Set Specific

Opcode	Command description
80h	Format NVM
81h	Security Send
82h	Security Receive

NVM Commands

Opcode	Command description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

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11. Certifications



EN 55022:2010

EN: 55024:2010

EN 61000-3-2:2013

EN 61000-3-3:2014

47 CFR, Part2, Part15, CISPR PUB.22

With reference to RoHS Directive 2011/65/EU recasting 2002/95/EC

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12. Ordering information

Series	*Model Name	Capacity	Flash	Length
Enterprise M.2 110mm PCIE SSD	E110PCIXTMLC-240G	240GB	NAND MLC	110mm
	E110PCIXTMLC-480G	480GB	NAND MLC	110mm
	E110PCIXTMLC-960G	960GB	NAND MLC	110mm

*XT refers to temperature range, ST refers to standard temperature, CT refers to enterprise temperature.

13. Contact Information

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